IN THE CLAIMS:

Please cancel claims 21-25, 32 and 35 without prejudice or disclaimer, and amend claims 1, 2, 7, 11-13, 17, 19-20, 26, 28-31, 33-34 and 36 as follows.

1. (Currently Amended) A method ~~for synchronizing a receiver to a transmitter ,~~ comprising:

receiving, by a~~the~~ receiver, a phase difference information indicating a phase difference between an internal clock and an external clock;

generating, by the receiver, a clock signal dependent on the transmitted phase difference information

generating, by the receiver, an internal clock or recovering an internal clock of a~~the~~ transmitter from information received from the transmitter;

frequency-dividing, by the receiver, the internal clock;

~~adjusting, by the receiver, the phase of the frequency-divided clock based on the received phase difference information;~~

storing, by the receiver, at least two successive values of the phase difference information received from the transmitter; ~~and~~

detecting, by the receiver, a difference between the successive values of phase difference information; and

adjusting, by the receiver, the phase of the frequency-divided clock based on the detected difference.

2. (Currently Amended) The method according to claim 1, wherein the internal clock and the external clock are frequency-divided within the transmitter to the same frequency, the method further comprising ~~the step of~~ converting the phase difference between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

3. (Previously Presented) The method according to claim 2, further comprising applying pulses of the frequency-divided clocks to start and stop inputs of a counter which generates the numerical value to be transmitted to the receiver.

4. (Previously Presented) The method according to claim 1, further comprising transmitting the phase difference information to the receiver in the form of multicast packets.

5. (Original) The method according to claim 1, wherein the internal clock is a symbol clock of 80 MHz or 89.6 MHz, and the external clock is an external clock reference of 2.048 MHz or 1.544 MHz.

6. (Cancelled)

7. (Currently Amended) The method according to claim ~~6~~1, further comprising multiplying, by the receiver, the frequency of the adjusted frequency-divided clock for generating an external clock.

8. (Previously Presented) The method according to claim 7, comprising including, by the receiver, a clock generator stage for generating the external clock, the clock generator stage comprises a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibiting the first counter from further counting when reaching a preset value.

9. (Previously Presented) The method according to claim 1, comprising:

selecting, by the receiver, depending on the difference between the successive values of phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

10. (Previously Presented) The method according to claim 1, comprising:

suppressing, by the receiver, depending on the difference between the successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

11. (Currently Amended) A system ~~for synchronizing a receiver to a transmitter, the system comprises~~ comprising:

a transmitter comprising a phase difference information ~~generating unit~~generator configured to generate phase difference information indicating a phase difference between an internal clock and an external clock, and a ~~transmitting unit~~transmittor configured to transmit the phase difference information to the receiver; and

a receiver comprising a ~~receiving unit~~phase receiver configured to receive a phase difference information indicating a phase difference between an internal clock and an external clock, a clock generator ~~unit~~ configured to generate a clock signal dependent on the transmitted phase difference information, a ~~generating unit~~generator configured to generate an internal clock or recover the internal clock of the transmitter from information received from the transmitter, a frequency-divider ~~dividing unit~~ configured to frequency-divide the internal clock, ~~an adjusting unit configured to adjust the phase of the frequency-divided clock based on the received phase difference information,~~ a ~~storing unit~~storage configured to store at least two successive values of the phase difference information received from the transmitter, ~~and~~ a ~~detecting unit~~detector configured to detect a difference between the successive values of phase difference information and an adjuster configured to adjust the phase of the frequency-divided clock based on the detected phase.

12. (Currently Amended) The system according to claim 11, wherein the transmitter further comprises:

a frequency divider ~~unit for~~ configured to frequency ~~dividing~~ divide the internal clock and the external clock to the same frequency; and

a ~~converting unit~~converter configured to convert the phase difference between the frequency-divided clocks to a numerical value to be transmitted to the receiver.

13. (Currently Amended) The system according to claim 12, wherein the ~~converting unit~~converter comprises a counter which generates the numerical value to be transmitted to the receiver, the counter having start and stop inputs to which pulses of the frequency-divided clocks are applicable.

14. (Original) The system according to claim 11, wherein the phase difference information is transmitted to the receiver in the form of multicast packets.

15. (Original) The system according to claim 11, wherein the internal clock is a symbol clock of 80 MHz or 89.6 MHz, and the external clock is an external clock reference of 2.048 MHz or 1.544 MHz.

16. (Cancelled)

17. (Currently Amended) The system according to claim 11~~16~~, wherein the receiver further comprises a ~~multiplying unit~~multiplier configured to multiply the frequency of the adjusted frequency-divided clock for generating an external clock.

18. (Previously Presented) The system according to claim 17, wherein the receiver further comprises a clock generator stage configured to generate an external clock,

wherein the clock generator stage comprises a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibiting the first counter from further counting when the first counter reaches a preset value.

19. (Currently Amended) The system according to claim 11, wherein the receiver further comprises:

a selector ~~unit~~ configured to select, depending on the difference between the successive values of the phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

20. (Currently Amended) The system according to claim 11, wherein the receiver further comprises:

a suppressor ~~suppressing uni~~ configured to suppress, depending on the difference between the successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

21-25. (Cancelled)

26. (Currently Amended) An apparatus ~~receiver used in a system for synchronizing a receiver to a transmitter, wherein the transmitter comprises a phase difference generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock and means for transmitting the phase difference information to the receiver, the receiver~~ comprising:

a receiver ~~receiving unit~~ configured to receive a phase difference information indicating a phase difference between an internal clock and an external clock;

a clock generator ~~unit~~ configured to generate a clock signal dependent on a phase difference information transmitted from a transmitter;

a generator ~~generating unit~~ configured to generate an internal clock, or to recover the internal clock of the transmitter from information received from the transmitter;

a frequency-~~dividing unit~~divider configured to frequency-divide the internal clock;

~~an adjusting unit configured to adjust the phase of the frequency-divided clock based on the received phase difference information;~~

storages for storing at least two successive values of the phase difference information received from the transmitter; ~~and~~

a detector ~~unit~~ configured to detect a difference between the successive values of the phase difference information; and

an adjuster configured to adjust the phase of the frequency-divided clock based on the detected difference.

27. (Cancelled)

28. (Currently Amended) The apparatus~~receiver~~ according to claim 26, further comprising a multiplier~~multiplying unit~~ configured to multiply the frequency of the adjusted frequency-divided clock for generating an external clock.

29. (Currently Amended) The apparatus~~receiver~~ according to claim 26, further comprising a clock generator stage configured to generate an external clock, the clock generator stage comprises a first counter for counting, in a round-rotating manner, a high frequency signal, and a second counter for counting the number of rounds of the first counter, the second counter inhibits the first counter from further counting when the first counter reaches a preset value.

30. (Currently Amended) The apparatus~~receiver~~ according to claim 26, comprising:

a selector ~~unit~~ configured to select, depending on the difference between the successive values of the phase difference information, one of the stored values of the phase difference information for adjusting the phase of the frequency-divided clock.

31. (Currently Amended) The receiver according to claim 26, comprising:

a suppressor~~suppressing unit~~ configured to suppress, depending on the difference between the successive values of the phase difference information, generation of a second pulse within one period of the frequency-divided clock.

32. (Cancelled)

33. (Currently Amended) A method, ~~for synchronizing a receiver to a transmitter wherein the transmitter generates phase difference information indicating a phase difference between an internal clock and an external clock, the method~~ comprising:

receiving, by ~~the~~ a receiver, a phase difference information indicating a phase difference between an internal clock and an external clock;

generating, by the receiver, a clock signal dependent on a ~~transmitted~~ received phase difference information indicating a phase difference between the internal and the external clock of the transmitter, the phase difference information being received from the transmitter;

generating, by the receiver, an internal clock or recovering the internal clock of the transmitter from information received from the transmitter;

frequency-dividing, by the receiver, the internal clock;

~~adjusting, by the receiver, the phase of the frequency-divided clock based on the received phase difference information;~~

storing, by the receiver, at least two successive values of the phase difference information received from the transmitter; ~~and~~

detecting, by the receiver, a difference between the successive values of phase difference information; and

adjusting, by the receiver, the phase of the frequency-divided clock based on the detected difference.

34. (Currently Amended) A system ~~for synchronizing a transmitter and a receiver, the system~~ comprising:

a transmitter comprising a phase difference information generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock, and transmitting means for transmitting the phase difference information to the receiver; and

a receiver comprising a receiving means for receiving a phase difference information indicating a phase difference between an internal clock and an external clock, a clock generator means for generating a clock signal dependent on the transmitted phase difference information, generating means for generating an internal clock or recovering the internal clock of the transmitter from information received from the transmitter, frequency-dividing means for frequency dividing the internal clock, ~~adjusting means for adjusting the phase of the frequency-divided clock based on the received phase difference information,~~ storing means for storing at least two successive values of the phase difference information received from the transmitter, ~~and~~ detecting means for detecting a difference between the successive values of phase difference information and adjusting means for adjusting the phase of the frequency-divided clock based on the detected difference.

35. (Cancelled)

36. (Currently Amended) An apparatus. ~~receiver used in a system for synchronizing a transmitter and a receiver, wherein the transmitter comprises a phase difference~~

~~generating means for generating phase difference information indicating a phase difference between an internal clock and an external clock and means for transmitting the phase difference information to the receiver, the receiver~~ comprising:

a receiving means for receiving a phase difference information indicating a phase difference between an internal clock and an external clock;

a clock generator means for generating a clock signal dependent on the transmitted phase difference information;

generating means for generating an internal clock or recovering the internal clock of the transmitter from information received from the transmitter;

frequency-dividing means for frequency dividing the internal clock;

~~, adjusting means for adjusting the phase of the frequency-divided clock based on the received phase difference information;~~

storing means for storing at least two successive values of the phase difference information received from the transmitter; ~~and~~

detecting means for detecting a difference between the successive values of phase difference information and

adjusting means for adjusting the phase of the frequency-divided clock based on the detected difference.